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DEPARTMENT OF ELECTRICAL ENGINEERING

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ENGINEERING DESIGN: ELECTRICAL ENGINEERING

REPORT 3: Final Report

ΒY

GROUP 5

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Name	Student number	Signatures	Dates
Evans Tjabadi	TJBEVA001	tteja badi	15/10/2018
Zayd Arnold	ARNZAY001	MA	15/10/2018
Nolundi Thomas	THMNOL002	Aur	15/10/2018
Lionel Arestide- Mangani	ARSLIO001	link	15/10/2018
Tanaka Zimuto	ZMTTAN001	Findo	15/10/2018

THE GROUP MEMBERS' INDIVIDUAL WORK REPORT (CONTRIBUTION)

1. EVANS TJABADI:

Worked mainly on the system **implementation and prototyping.** Did some of the work on SPI communication and integrated the normal **PWM code** into it. Presented some of the **system level testing results** and worked on the helped with the general formatting of the report.

2. ZAYD ARNOLD:

Focused more project **implementation** and **testing**. Wrote the **Arduino code** for the PWM, this was used for the 1st prototype. Assessed the **user requirements** and analysed them. I conducted research on different types of components (particularly those that affect the sub-systems significantly) that would best fit the design of the switch mode power supply. I found **recommendations** that would could improve the project and possibly simply it in the future.

3. NOLUNDI THOMAS:

Came up with **design approach 3** with typed explanation on how it functions, ccompleted calculations for the **duty cycles** of the two load requirements, designed the overcurrent **protection circuitry** of the system and sourced some components (from calculated component values) to populate the **Bill of Materials**. **Compiled** and **integrated** report findings for final submission of project.

4. LIONEL ARESTIDE-MANGANI:

Did some work on the display interface(minimum) to be combined with the main SPI code. Mainly worked on the formatting of the report and research and recommendations of components (mainly the rectifiers and filter components to be used in one of the design approaches) for the compilation of the bill of materials.

5. TANAKA ZIMUTO:

Came up with one of the design approaches (design approach 1). I also analysed the **user requirements** and came up with the **technical requirements** list. I also drew the **functional tree**. I also had to investigate the effect of using a **transformer** and at which stage should we put it. Selected the switching **MOSFET** that we bought. Helped to compile **final report**.

EXECUTIVE SUMMARY

This report aims to show the step by step procedure in the design and implementation of a switch mode power supply, which will be used to supply current to various loads and systems. This will cover the initial problem case, the translated problem case to system requirements and the design of the Switch Mode Power Supply (SMPS), which involves many possible solutions being simulated and compared against each other and the best solution will be selected for implementation and prototyping of the device. The prototyping phase will involve the implementation of the desired method, which will involve some modifications to the original design, problems faced during construction and work around to those problems faced as well as the individual sub-system test. Finally, the report presents the test of the entire system and discusses/compares the output with the required output and also analyses variances and any possible causes for the variances observed and recommends actions for system improvement.

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1. INTRODUCTION

Power supplies play a very important role in our daily lives. The power suppliers are the core of almost every device ranging from huge industrial equipment to miniaturized devices. Due to their applications (which might be very critical like in medical/clinical equipment), these devices should provide power with very high reliability and efficiency and low-down run-time.

The purpose of this project is to describe the design process undertaken to build a Switch Mode Power Supply (SMPS). The report will start off with a description of the user and technical requirements, and then the performance goals and test protocols which will be used for the acceptance test of the designed system. Multiple design approaches will be shown with emphasis on different functional benefits, taking into consideration the constraints of the design. One design will be chosen for implementation based on a discussion on comparison of the different designs presented. Part of the comparison will also include an investigation into the chosen design systems' performance against the desired technical requirements using simulation techniques on MATLAB Simulink.

The report details the calculations of the system components values and their voltage and/or current operating requirements. The report goes into depth as to why certain components where picked over others and motivates the circuits choices. The bill of materials for the SMPS system with the final selected components is prepared and compiled at the end of the report. The report concludes with the practical implementation of the system and the performance result during laboratory testing.

Finally, in the report we will show the logical integration of the working sub-systems and how their integration was tested for successful realization of the system and user requirements.

2. PROBLEM STATEMENT

A user has approached the group with a requirement. The user desires to have an SMPS system with a friendly interface. The user wants to choose between 5 V and 9 V from the interface and the system should be able to provide currents from 0 A to 1 A. The system should use microcontrollers to control the operation of the system and should provide high quality power.

3. THEORETICAL BACKGROUND

A power supply is an electronic circuit that is used to provide electrical power to appliances or loads. These loads require various forms of power at different ranges and with different characteristics. For that reason, power is converted into the required forms with the desired qualities by using some power electronic devices or converters. Electrical and electronic loads work with various forms of power supplies, and for this project our investigation delves into the design and implementation of a Switch Mode Power Supply.

What is a Switch Mode Power Supply (SMPS)?

It is an electronic power supply integrated with the switching regulator for converting the electrical power efficiently from one level to the other with desired characteristics. It is used to obtain regulated DC output voltage from unregulated AC or DC input voltage. Basically, an SMPS is a device in which energy conversion

and regulation is provided by power semiconductors that are continuously switching on and off at a high frequency. SMPS's are used in many applications as an efficient source of power, plus having the added advantage in terms of size, weight, cost, efficiency and overall performance.



Figure 1: Block Diagram of a typical SMPS

The above block diagram represents the inner blocks of a typical SMPS. The high voltage AC is first stepped down using a transformer, then rectified and filtered. The filter output DC voltage is then stepped down to the desired level using a high frequency switching system - Buck converter. The output of the buck converter is feed to the load. Current limiter and feedback loop circuits can be added to regulate the current and voltage actively.

SCOPE AND LIMITATIONS OF THE PROJECT

The project only focuses on designing and building a switch mode power supply. The SMPS is designed to provide only +5 V and +9 V and a current of only up to 1 A.

While there are many other power supply designs like the linear power supply design, this project only focuses on the switch mode power supply (SMPS) topologies.

4. PURPOSE OF THE REPORT

The report intends to outline the design and implementation process of an SMPS system. The report analyses user and technical requirements for efficient design and implementation. The report also presents the system level performance of the final product.

5. USER REQUIREMENTS

User Requirement Analysis

The switch mode power supply (SMPS) will be plugged directly into a mains outlet, thus it will receive an input AC voltage of 230 V_{rms} at a frequency of 50 Hz. It is required for the system to produce a DC output voltage of either 5V or 9V, depending on the user's desire. There are 2 methods of arriving at a DC output voltage of 5/9V given an AC input voltage of 230 V_{rms} :

- Connect the input voltage to a transformer and then step down the voltage to either 5V or 9V. Bearing in mind that this voltage is still AC it will need to be converted to DC, which can be done using a rectifier. This rectified voltage will thereafter be connected to a voltage regulator.
- 2. In the second method the initial process is flipped. The input voltage will be filtered and then converted to DC using a rectifier including a capacitor. The filtering of the input voltage will serve as to remove any undesirable irregularities in the waveform. The rippled voltage at the output of the rectifier will pass through a voltage regulator to ensure that the voltage being supplied to the variable load is indeed constant. This voltage will now need to be stepped down to 5/9V. This can be done using a step-down DC-DC converter.

Given that no transformers may be used in the design of the SMPS method 1 will be abandoned and method 2 will be executed in the design process of the SMPS. Similarly, the commercially available linear voltage regulators cannot be used in the design of our SMPS, thus the voltage regulators included in the design will be built using discrete components.

The SMPS will need to produce a current ranging between 0 A and 1 A. The value of the desired current output will also be user-set. Some protection circuitry in the form of a current limiting circuit will need to be included to ensure that the SMPS does not produce a current that exceeds the set current even if there is a short circuit at the load.

The next requirement is physical and states that the connecting cable or wire may not breach a length of 1m.

The load to which the SMPS will supply will be variable and it is required that the current must be set from 0 A - 1 A, thus voltage and current must change in order to meet this requirement.

Technical Requirements

- Less than 1 m distance between the load and the SMPS for less output voltage distortion.
- An intelligent load (digital potentiometer) controlled by an STM32f0 board to vary currents.
- Continuous SPI communication between interface and supply microcontrollers.
- Current and voltage will be changed by the supply microcontroller using PWM with interface microcontroller commands.

- The rating of the switch and other components in the high voltage circuit should have rating which are considerably above an AC voltage of 300 V to ensure that they do not burn.
- The desired output voltage will also be obtained simply by pressing a push button on the microcontroller. To get the desired output voltage the PWM will change the duty cycle so that the 5V or 9V will be obtained.
- Current should be selected using a potentiometer user friendly interface required.

Functional Tree Requirement

The following diagram shows the requirements tree of the developed technical requirements for the systems operations.



Figure 2: Functional Requirements Tree

6. POSSIBLE CONSTRAINTS AND CHALLENGES

- Usage of either low or high frequency transformer is not advised. The buck converter must step down the AC mains voltage (230 Vrms) to 5/9 V using a PWM.
- The mains voltage is relatively high for discrete electronics, high voltage tolerant components should be used for the rectifier, filter and the buck converters.

- Having resistors in parallel (with control switches) can only make the load be able to sink in discrete levels of currents and not the whole 0 1 A spectrum.
- Since it requires several components as well as many circuits in it at various stages, fitting these in a limited space might become very difficult.
- Since the initial stages work at above an AC voltage 300 V and the mains may not have a robust protection circuitry (or cut at a higher current limit), any unnecessary short circuits may cause damages in the components.
- The cost of the design and implementation may not exceed the user's set limit. No expensive components or extra components used unnecessarily
- Usage of mechanical controls for load variations could increase response times and add mechanical losses.

7. PERFORMANCE METRIC GOALS FOR THE SYSTEM

- The output voltage and current should be within 2% accuracy.
- The output voltage and current ripples of less than 5%.
- Maximum output current should not be more than 5% greater than the 1 A limit.
- Total processing time of less than 0.5 seconds.
- THD and TDD of the output voltage and current should less than 5% at full load.

8. ACCEPTANCE TEST PROTOCOLS

- Request for supply voltage of +5 V at no load and measure the actual output voltage after 0.5 seconds of request. The actual output voltage should be within accuracy of 2%, have a THD of less than 5%, and a ripple of less than 5%.
- Request for supply voltage of +9 V at no load and measure the actual output voltage after 0.5 seconds of request. The actual output voltage should be within accuracy of 2%, have a THD of less than 5%, and a ripple of less than 5%.
- Request a supply current of 0.2 A at +5 V and then measure the actual output current and voltage. The accuracy of the current and voltage should be within 2%, and the TDD and THD should be less than 5%. The current and voltage ripples should be less than 5%.
- Request a supply current of 0.6 A at +9 V and then measure the actual output current and voltage. The accuracy of the current and voltage should be within 2%, and the TDD and THD should be less than 5%. The current and voltage ripples should be less than 5%.
- At +5 V voltage supply. Increase the load beyond the allowed maximum (1 A) to 3 Ω and then measure the output current of the supply. The protection circuitry should limit the current to only 1A with an accuracy of 5%.

 At +9 V voltage supply. Increase the load beyond the allowed maximum (1 A) to 3 Ω and then measure the output current of the supply. The protection circuitry should limit the current to only 1A with an accuracy of 5%.

9. POSSIBLE IMPLEMENTATIONS

Design Approach 1



Figure 3: The block diagram of design approach 1.

The AC power from the main is rectified to a pulsating DC voltage and the filtered. A buck converter is used to step the DC voltage down to the required 5 V or 9 V using a PWM signal from the supply microcontroller ($V_{Load} = DV_{in (Buck)}$). The supply microcontroller monitors the output voltage and adjust the duty cycle to make any adjustments when necessary.

The user interface is controlled by the load microcontroller. The load microcontroller sends information about the supply voltage and current to the supply microcontroller, which sends signals to change the operation of the supply system to meet the load requirements. The user interface has LCD screen to display the desired and actual voltage and current levels. The load microcontroller adjusts the load to be able to sink in the selected currents and a selected voltage.

The load had an extra port to add an external load. The current limiter operates to limit the current to 1 A if the load tends to draw more.

Design Approach 2



Figure 4: The block diagram of design approach 2

The first rectifier stage will convert the AC signal to a half wave signal which will be driven to the transformer by the switch. A high voltage MOSFET can be used for the switch. From the secondary side of the transformer the signal is converted to a DC voltage which passes through a filter and then to the load.

The isolation is created by the combination of the tiny switch mode transformer and the regulator which will be designed. The designed regulator will also carry the feedback voltage back to the primary side.



Design Approach 3

Figure 5: The block diagram of design approach 2

This design approach is similar to approach 1 described above with the difference that instead of using one buck converter, two are used and a voltage regulator incorporated between the converters. The reason for using 2 converters is to ensure the realisation of a realistic duty cycle by using a 2-stage step-

down conversion process. The voltage regulator ensures that there are less ripples and a steadier output is realised from the first converter since it will be stepping voltage down from 325V to an intermediate voltage of around 30Vpp.

Comparison and Choice of Design

Transformer (or lack thereof):

The major difference in the two design approaches above is the inclusion of a transformer. The transformer comes with its advantages in that it will step down the voltage to a reasonable value (probably to around 30 V) thus making the design of the buck converter a lot easier, also values obtained are more assured. However, the transformer will cause harmonics and thus high distortions in the output. They are also limited to the manufactures specifications hence we cannot make any alterations to the device when required. Hence, we decided to opt for design option 1.

Rectifier:

There were a few options of rectifier types to choose from, namely a full bridge, half bridge and thyristorcontrolled rectifier. A full bridge rectifier is chosen against a half bridge and a thyristor-controlled rectifier for this design of the SMPS. Compared to the full bridge rectifier the half bridge rectifier has a lower efficiency. This is so because that it does not conduct in the reverse cycle. The thyristor-controlled rectifier adds extra components to the system and due to budgetary constraints, an increase in build costs is to be avoided

Switch:

Choices of a switch controlled by PWM in the DC-DC converter were that of a MOSFET, IGBT and BJT. Compared to an IGBT a MOSFET has a lower gate-to-drain feedback capacitance and a lower thermal impedance. The lower thermal impedance means less heat loss and thus less power loss. This in turn makes for a more efficient switching device. THE MOSFET also produces lower rise and fall times which facilitates better switching at high frequencies ^[3]. It is for these reasons a MOSFET would be better fit than an IGBT.

Between a MOSFET and a BJT, a MOSFET can operate at much higher frequencies and have much higher input impedance than a BJT^[2]. A MOSFET is also more efficient because less power is dissipated during switching ^[4]. Therefore, a MOSFET was chosen against the normal BJTs to operate as a switch in the buck converter subsystem.

Filtering system

The decision taken for the filtering system required for this system implementation was based on simplicity and on which method would be more cost effective. Placing two big capacitors across the output proves to satisfy both those requirements. The capacitors used in this system are two 1000 μ F capacitors rated at 450 V.

Converter type:

Since the systems operates from the mains, and the goal is to step down the voltage to the desired levels, hence only step-down converters are necessary. Consequently, a buck converter would be better fit as opposed to a buck-boost converter as the facility to step up the voltage in the buck-boost converter is

unnecessary. A CUK converter is a buck converter cascaded with a boost converter and operates similarly to a buck-boost converter in that in can perform as a step down or step up converter. Therefore, the buck converter was the DC-DC converter of choice compared to the buck-boost and CUK converters because it only steps down voltage and therefore has less components. Other options for converters included isolated converters, but these converters include transformers in their design and were thus disregarded completely.

Sub system requirements

- **RECTIFIER:** A full bridge voltage rectifier is required to convert the AC mains into a pulsating DC voltage. The diodes should be able to handle the mains peak to peak voltage (> 320 V) and the maximum current, even taking into consideration situations where current exceeding the set limit were to be drawn.
- **FILTER CAPACITOR:** The filtering capacitor should be a high voltage (350 V) tolerant and have a much higher value (>1000 F) to smoothen out the pulsating DC voltage from the rectifier.
- **BUCK:** The main purpose of this is to step down the unregulated voltage from the rectifier to the required voltage be it 5 V or 9 V. The circuit will consist of inductors and capacitors, as well as a MOSFET switch to achieve this task. The output voltage is related to the input voltage by V Load=DVin (Buck)
- , where the "D" is the duty cycle of the PWM. For example, to get 5 V out of a 320 V (peak of the rectifier tracked by the capacitor), the duty cycle becomes 1.56 %.
- **CURRENT:** A robust current limiting circuit made of transistors and resistors will be used to achieve a current limit of 1A at the output and have very minimal voltage (< 0.2 V) drop across itself.
- **MICROCONTROLLER 1**: This will be used as the PWM driver and central controller for all operations. It will be responsible for monitoring current flowing as well as changing the duty cycle on the buck converter for the required voltage. This will be the heart of the entire system. An Arduino development board is considered for the PWM driver for its usage simplicity.
- **MICROCONTROLLER 2:** This will control the interface between the user and the system (the PWM driver). The user will input what they require from the system and this microcontroller will communicate this to the driver. An STM32f0 is considered to manipulate the load resistances.

Choice of Design

The design approach 3 was chosen for implementation in this project. The main focal point of the design is that it uses a two stage DC-to-DC step down system in conjunction with a voltage regulator. The voltage regulator will be placed between the two Buck converters. The purpose of this is so that the voltage regulator will smoothen out the output voltage received from the stage 1 buck converter. This voltage will then be stepped down further to either 5V or 9V by the stage 2 buck converter. This process will ensure an overall more constant and stable supply voltage to the load.

10. RESULTS OF THE DESIGNED SYSTEM SIMULATION

The SMPS designed with two buck converters.

It was investigated and concluded that an SMPS using only one buck converter and no low frequency transformer before the rectifier circuit is very sensitive to slight changes in the duty cycles. To reduce costs and avoid power quality problems, two buck converters were used in cascade mode as can be seen in Figure 6.



Figure 6: Two stage buck converter

The output voltage and current results

Unfortunately, the system behavior shows undesirable performance. The input impedance of a buck converter is highly dynamic, and when two buck converters are operated in cascade mode, loading effects occurs.

The following figures show the undesirable results from the system. Fig.2 and Fig.3 show the results when an output voltage of 5 V is requested with an output current of 1 A. Fig.4 and Fig.5 show the results when 9 V is requested at 1 A. Both results below are undesirable.

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Figure 7: Voltage results at 5V & 1A



Figure 8: Current results at 5V & 1A

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Figure 9: Voltage results at 9V & 1A



Figure 10: Current results at 9V & 1A

Despite the undesirable behavior of the designed system, the simulations results show that system reduces the ripple content significantly and that the system has a reduced sensitivity to little changes in the duty cycles. The following figures show the results when the duty cycles are varied slightly.



The above results figures show that a 0.1% change in the duty cycle only changes the voltage from 5.0001 V to 5.00285 V, therefore the sensitivity to duty cycle slight changes has been reduced. The ripple voltage in both is 150 μ V.

11. MOTIVATION FOR A NEW DESIGN

The system performance is outside the acceptable limits of the user's desires and the technical requirements of the system. Though the system achieves ripple content of less than 0.0026 %, the produced output parameters reach an error of more than 2 % at the highest current desired. The voltage and current overshoots during the transient period are more than twice the required values. This system behavior is unacceptable according to the Acceptance Test Protocols (ATPs) clearly outlined in the user's and technical requirements report, hence the design is rejected and a call for a new better performing system is made.

12. THE REVISED SYSTEM DESIGN

The following figure shows the revised SMPS system. The design only uses one buck converter system. The voltage from the main is first rectified, filtered and then stepped down to the desired value using only one buck converter.



Figure 13: Revised SMPS Design

13. THE REVISED TECHNICAL SPECIFICATIONS

From the analysis of the user's requirements, the technical specifications of the system and the subsystems were formulated as following:

- The user can choose between 5 V and 9 V output voltages using an interface.
- The user can select any desired current value between 0 A and 1 A at either 5 V or 9 V.
- The system should produce desired output voltage with less than 2 % error, less than 5 % ripple content and less than 5 % total harmonic distortion (THD).
- The system should produce desired output current with less than 2 % error, less than 5 % ripple content and less than 5 % total demand distortion (TDD).
- The voltage and the current voltage overshoots during the transient period should be less than 50 % of the required parameters.

14. SYSTEM CALCULATIONS

The duty cycles

- The voltage drop across each of the diodes is 0.8 V.
- The voltage drop across the switch is 1.5 V.
- The output of the voltage rectifier with the filter has a mean of 324.29 V.

$$D = \frac{V_{out} + V_d}{V_s - V_m + V_d} \times 100\%$$

 \circ The duty cycle for the 5V output:

$$D_{5V} = \frac{5 + 0.8}{324.29 - 1.5 + 0.8} \times 100\% = 1.7924\%$$

• The duty cycle for the 9V output:

$$D_{9V} = \frac{9 + 0.8}{324.29 - 1.5 + 0.8} \times 100\% = 3.0285\%$$

The inductor value

$$L = \frac{(V_{in} - V_{SW} - V_{OUT})(V_D + V_{OUT})}{(V_{in} - V_{SW} + V_D)f_{SW}rI_{out}}$$

Where r is chosen to be 0.3. The maximum load of 1 A is used for lout.

For the 5 V output voltage:

$$L = \frac{(324.29 - 1.5 - 5)(0.8 + 5)}{(324.29 - 1.5 + 0.8)(20000)(0.3)(1)} = 949.3 \ mH$$

For the 9 V output voltage:

$$L = \frac{(324.29 - 1.5 - 9)(0.8 + 5)}{(324.29 - 1.5 + 0.8)(20000)(0.3)(1)} = 937.4 \ \mu H$$

As the inductor value increases, the ripple factor decreases. Though bigger inductors reduce the ripple content, bigger inductors may be impractical. The inductor value is chosen to be 1000 μ H which is the nearest E12 value.

The buck converter capacitor value

- The MOSFET switches at a frequency of 20 kHz.
- ΔV_{out} = 5.005 4.998 = 0.007 V.
- $\Delta I_{out} = 1.005 0.005 = 0.01 A.$

The minimum capacitor needed to get the above ripples given by:

$$C_{min} = \frac{\Delta I_{out}}{8f_{SW}\Delta V_{out}} = \frac{0.01}{8 \cdot 20000 \cdot 0.007} = 8.9 \,\mu F$$

The minimum capacitor needed to prevent voltage overshoot is:

For
$$V_{os} = 0.01 V$$

$$C_{min} = \frac{\Delta I_{out}^2 L}{2 \cdot V_{out} \cdot V_{os}} = \frac{0.01^2 \cdot (1 \cdot 10^{-3})}{2 \cdot 5 \cdot 0.01} = 1 \,\mu F$$

A 10 µF capacitor was chosen for the buck converter capacitor. A bigger capacitor reduces the ripples.

TDD and THD calculations

The ripple of the output can be modelled as a triangular wave. To find the harmonics within this wave the Fourier coefficients of the wave can be calculated using the formula below.

$$b_n = \frac{8}{\pi^2 n^2} \begin{cases} (-1)^{\frac{n-1}{2}} & \text{for } n \text{ odd} \\ 0 \text{ for } n \text{ even} \end{cases}$$

The THD can be calculated using the formula

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \cdots}}{V1}$$

The TDD can be calculated using the formula

$$TDD = \frac{1}{I_L} \sqrt{\sum_{n=2}^{M} I_n^2}$$

FFT analysis was performed using Simulink where the harmonics can be seen in the frequency domain.



Figure 14: Simulink simulation FFT analysis for 5V



Figure 15: Simulink simulation FFT analysis for 9V

15. THE CURRENT PROTECTION CIRCUITRY

For the system over-current protection, a simple current limiter was chosen for implementation as seen in Figure 14 below.



Figure 16: Current limiting circuit

 R_{sense} is the resistor used to select the maximum current which needs to flow to the load, which is 1A for this design. Using the equation V = IR, we were able to calculate the value of Rsense to be 0.8 Ω .

16. THE COMPLETE SYSTEM DESIGN CIRCUIT

The complete system design was put together in LTSpice software.



Figure 17: Complete integrated system design

17. THE VALUES AND TOLERANCES OF SUBSYSTEMS COMPONENTS

The rectifier and the freewheeling Diodes

A 1N5395 diode will be used. This is a 450 V general purpose diode. The average current rectified is 1.5 A.

Filtering capacitors

The filter capacitors smoothening the rectifier output voltage should be as big as possible (as the budget allows). Two 1000 μ F through-hole electrolytic capacitors with 10% tolerance are desired for this SMPS system. The capacitors should be able to handle voltages above 350 V (or at least peak of the mains supply voltage).

The switch (MOSFET)

A 400 V IRF740BBRF through-hole MOSFET will be used. The voltage drop across the MOSFET is 1.5 V and internal resistance is 0.5 Ω .

Inductor

The value of the buck converter inductor is 1 mH with a tolerance of 10 %. The inductor should have a current rating greater than 1 A. The inductor should be a through-hole component for ease of system integration.

Buck Converter capacitor

The value of the buck converter capacitor is $10 \ \mu$ F with a tolerance value of 10%. The capacitor must be able to handle more than 20 V (or at least more than the desired output voltages).

The current protection

For the current protection circuitry, two transistors and two resistors will be used. The transistors that will be used are NPN type BJT's which are able to handle more than 1 A of current. The resistor values that are used are 100 Ω (R) and 0.8 Ω (R_{sense}).

<u>Microcontroller</u>

The microcontrollers that will be used in our system are the STM32F0 and Arduino Uno. The STM32F0 will be used as the user interface and communicate with the Arduino to generate the PWM which will then alter the duty cycle of the buck converter to which ever percentage depending on the output voltage desired by the user.

18. FUNCTIONALITY TESTING OF EACH SUB-SYSTEM

Subsystem Test Simulations

AC/DC converter [Rectifier and Filter]



Figure 18: The rectifier system output voltage.

The results when 5 V is selected at currents (1 A and 0.5 A).

			- 22	F * Signal Stat	istics	йX
				Max Min Peek to Peak Mesan Mesian RMS	Volua 5.060.e+00 4.883e+00 1.765e-01 4.957e+00 4.853e+00 4.557e+00	Time 1.865 1.255
12	16	i.				

Figure 19: 5V at 0.5 A system results.

		🕮 👎 🛪 Sign	al Statistics * ×
		Max	1.012e+00 1.865
		Min	
		Magn	9.8744-01
1		Medan	9.780e-01
		RMS .	9.876e-01
		No.	Marcal I
6.6	28		
84			
62			
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				Signal Statistics
				A CONTRACTOR OF A CONTRACTOR
				Mar 51928100 0.945
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				Pesk to Peak 1791e-01
10	and the second	States - States - States - States - States	in the second of the second second	Mpon 4.935e+00
A REAL PROPERTY AND A REAL				Marian & BRZeHOU
				Distr. I Diff. 100
				4.0356400
4				
1				
				12 C
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2				
D				

Figure 21: The output voltage when 5 V is requested at 0.5 A.





The results when 9 V is selected at currents (1 A and 0.5 A).

				181 ∓▼Signal	Statistics	× x
10				Nax Min Pesk to Fe	Value 9 103e+00 8 811e+00 ek 2 925e-01 8 890e+00	Time 2,155 2,405
				Median	9.023e+00 8.091e+00	
				-		
10						
	69	13	23			

Figure 23: The output voltage when 9 V is requested at 1 A.



Figure 24: The output current when 9 V is requested at 1 A.

		Ť.	<u>)</u>		Ð	* V Signal Sta	tistics	* ×
10						Max Min Peak to Paak Meteri Mediari RMS	Value 9.121e+00 8.027e+00 2.935e-01 8.935e+00 8.934e+00 8.934e+00	Time 0.685 2.625
Ŧ								
-5								
	55		*	3				

Figure 25: The output voltage when 9 V is requested at 0.5 A.

	T T Signal Statistic	oš /××
		/aloe Time:
	Max 5.0	1674-01 0.995
	Min 4.9	04e-01 2.525
	Desit to Deal 15	
89	Maan 20	MBa-01
		2400-01
	rixedian 4.3	SODE-UT
	1000 419	56(20-0)
84		
6.5		
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Figure 26: The output current when 9 V is requested at 0.5 A.

The output voltage of this SMPS is naturally controlled by the PWM. The challenge is protections is the current overload which to results from low resistance loads. The system protection circuit was simulated and tested in LTSpice. The Fig.20 shows a normal operation at 5 V and 1 A.



Figure 27: The current under normal operations.



Figure 28: The SMPS with an increased load.

The load resistance was decreased to increase the load demand. The Fig.21 shows the load resistance. The system is set to produce 5 V and initially set to produce 1 A. Fig.22 below shows the output current when the system is overloaded.



Figure 29: The results of the SMPS protection test.

In the simulation demonstration tests were performed to see how well the system would respond to loading. A screenshot of the Simulink simulation is shown below.



Figure 30: The systems response to loading

19. THE (INTELLIGENT) LOAD

The user choses a certain current at a certain voltage and the system should reconfigure the load characteristics to be able to sink in the current chosen by the user. The load then must be a variable load controlled by the load microcontroller while the supply microcontroller controls the maximum current the load can draw from the supply at each selected voltage. The load should be able to sink in currents between 0 A and 1 A at both output voltages, therefore the minimum resistance needed on the load system is 5 Ω (5 V at 1 A).

A digital potentiometer of $1 \text{ k}\Omega$ and 8 bits resolutions will be used for the load. The digital potentiometer has a step resistance of 3.9Ω , which is deemed sufficient for this project. The load microcontroller can be used to send digital signals to the digital potentiometer to set a resistance between two pins that would be able to sink in the chosen current. If necessary, discrete resistor could be added to vary the load further.

20. POSSIBLE ADD-ONS CIRCUITRY

Control feedback circuit:

The design current uses an open loop configuration. A closed loop control circuit can improve the results of the system. The output voltage is sampled frequently and the (down scaled) output is feed into the supply input pins. The sampled output is compared to the required output and according to the percentage difference, the duty cycle is changed accordingly to meet the desired output.

Voltage protection circuitry:

During the simulations of the systems, it was observed that the system does not respond very well to less loads (high resistive loads), this results in higher output voltages which are undesired. The control feedback circuit should be able to reduce this effect, but to make the system even more robust in terms of protection, an overvoltage protection system can be employed to shut down the load completely if the output voltage tries to increase.

Voltage regulator:

A linear voltage regulator might also be added depending on whether it will make a significant difference to the voltage output. It must be noted that this voltage regulator will be built using discrete components. It will also incur added cost, therefore should it not affect the output voltage significantly it will not be added.

21. THE PRACTICAL IMPLEMENTATION AND PROTOTYPING

SPI communication: Supply and Load Microcontrollers

The initial plan was to use the STM as an interface which will communicate with an Arduino to produce the PWM needed for the Buck converter. Either SPI or USART communication could be used for the microcontrollers. Information about communication between Arduino and STM was tough to find and even with limited information sourced it was seemingly difficult to implement SPI or USART between Arduino and STM. However sufficient information was found about SPI communication between two STM boards and this was thus successfully implemented. Therefore, two STM's were used, one for the user interface and the other to produce the PWM.

The user required a user-friendly interface to switch between voltages and to select voltage level and two microcontrollers for the interface and for the buck converter control. A successful STM32f0 to STM32f0 SPI communication has been set up to communicate commands from the interface to the supply controller. The supply microcontroller (slave) receives duty cycles from the master (interface microcontroller) and produces a PWM with the received duty cycle to drive the base of the switching device.

The figure below shows the two microcontroller sub-system in operation.



Figure 31:The SPI microcontroller sub-system.

Inclusion of Transformer

After the first prototype was built it was found that the system would operate more stably if the input voltage received from the mains was stepped down using a transformer from 230V to an intermediate voltage lying around \pm 20V and then fed onto the buck converter. In the prototype of our original design

where the transformer was not used the voltage supplied by the mains, 230V_{rms} was fed directly into the buck converter and then stepped down to either 5 or 9V. This proved problematic because the ripple implied by the buck converter was large and inconsistent in each testing.

Duty cycles

New duty cycles were calculated based on the new components added to the circuit and adjustments made. These new duty cycles were calculated as follows

$$D_{5V} = \frac{5 + 1.4 - 1(20 \times 10^{-3})}{\sqrt{2}(15) - 0.2 - 1(20 \times 10^{-3}) - 1}$$

= 35.01%
$$D_{9V} = \frac{9 + 1.4 - 1(20 \times 10^{-3})}{\sqrt{2}(15) - 0.2 - 1(20 \times 10^{-3}) - 1}$$

= 57.05%

BJT used in Buck converter

The use of the MOSFET for switching in the PWM was abandoned and replaced with the TIP31 BJT. This change was made because it was found that the voltage drop across the MOSFET was far greater than the anticipated 1.6V. With the inclusion of the MOSFET in the circuit the Buck converter was stepping down the voltage of 21V (from the DC power supply) all the way down to around 2V. For long it was unknown why this was happening until it the amplitude of the PWM was changed from 3.3V to 5V (on the signal generator). Once this change to the PWM was made the buck converter operated as expected and produced a voltage of 9.24V when tested for 9V. The need for the PWM amplitude to be 5V became a problem because the highest the STM's GPIO pins can produce is 3.3V. It was then decided that to test the BJT using

Sub-systems testing:

Each subsystem was tested under the conditions they are supposed to operate at. This serves as protection against the components used in the circuitry of subsequent sub systems. After each sub system was tested and found to operate as expected the full circuit was constructed.

Transformer, rectifier and filter circuit

The transformer was connected to the store-bought full bridge rectifier which was then connected to the two $1000\mu F$ capacitors. The capacitors will serve as the filter to smoothen the rectified AC voltage. The circuit is shown below



Figure 29: Transformer-rectifier circuit

Before connecting the transformer-rectifier combination to the supply values were calculated for the expected output.

Since the transformer was rated 230V/15V a multimeter reading of $15 \times \sqrt{2}$ will be expected for the V_{rms} at both ends of the capacitor. This will yield a voltage of 21.21V

The circuit was then connected to the Variac (variable autotransformer) which was then powered on and turned to 230V. The voltage recorded at the output of the circuit was 25.64V which shows that the circuit was thus working.

PWM

The PWM produced by the STM board was tested on the oscilloscope and is shown in the picture below. In this instance the frequency was set to 120 kHz and the duty cycle set to 3%. The output produced by the STM had an amplitude of 3.3V and oscillated between the peak and 0.



Figure 32: PWM testing on STM board

Buck converter

The buck converter was tested first by using the DC power supply as a sinusoidal input voltage of 21V. This was a safety precaution to protect not only the systems circuitry but also the equipment in Machines Lab. The PWM used for switching the BJT was set using the signal generator. The signal generator was set to produce a square wave at 120 kHz oscillating between 0 and 3.3V. The duty cycle was changed so that the buck converter would produce either 5 or 9V at the output.

A variation of 0.4V was accepted, this meant the output could be within $5V \text{ or } 9V \pm 0.2V$ to be acceptable. However, a voltage of above either desired voltage was intended. This was to account for any unforeseen voltage losses or voltage losses due to the effects of loading.

Interface implementation

The following figures below show the presentation of the implemented design. The interface uses the STM32f0 board. A welcome message is displayed upon system activation and option of 5 V and 9 V are







Figure 37: Welcome Message.



Figure 34: 9 V display.

Figure 36: Voltage Option.





Figure 33: Current selection.

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shown. Even though the system didn't implement current selection and control, the interface allows the user to select a desired current level with a potentiometer.

Protection circuitry

The protection circuitry was built using the intended design. This circuit was then tested in White lab however it was found that the DC power supply could not supply a current in excess of 1A. Therefore, we were not sure whether our current protection circuitry was working when a small resistor was made to be the load or if the DC power supply itself was limiting the circuit from drawing 1A. Consequently, the protection circuit was not added to the system. Instead a fuse was added so that the fuse would blow if a current greater that 1A was drawn

System Integration and Testing

The following figure below shows all the sub-systems of the SMPS integrated together for complete system test and display. The system has an easy to connect input and output end connection ports. The interface is quite friendly with push buttons to select voltages and a potentiometer to select current level.

The system was connected to a 230 V AC input voltage from a Variac (Variable autotransformer) and the output power parameters were measured, and the results are presented below.



Figure 39: The complete SMPS without the microcontrollers.

The figure below shows the 9 V low current testing before the system presentation.



Figure 38: Output voltage of the 9 V low current test.

The following figure shows the ripple analysis of the output voltage of 5 V.



Figure 40: The output ripple content analysis at 5 V

Fast Fourier Transform analysis was performed on the full buck converter on the oscilloscope. This is a frequency domain representation and the harmonics (vertical bars) can be seen to be decreasing as the frequency increases.



Figure 41: FFT analysis of the full buck converter for 5V



Figure 42:: FFT analysis of the full buck converter for 9V

22. CONCLUSIONS

The user requires a switch mode power supply which gives output voltages of +5 V or +9 V and a current between 0 and 1 A, and the SMPS is to be powered from the AC mains (230 V_{rms}).

Due to time limitations the SMPS was only tested at 5V and it produced an output of 4.5V, which is much closer to the required voltage. These variations where caused by the fact that we implemented a design with a BJT as a switch rather than a MOSFET, hence the larger voltage drop across the BJT and hence the difference in the voltage, but otherwise the voltage performance was acceptable.

The Currents flowing through the selected loads where supposed to be between zero and on, which was achieved as our current flowing through the load was around 0.03A or 30mA which is an acceptable amount to prevent damage to both the SMPS and the load itself.

Due to time constraints, some of the aforementioned features like the protection circuitry could not be implemented in the final device as well as accounting for an intelligent load, which could have improved our systems performance as well as reduced the risk of destroying some of the components.

Overall, our system generally managed to achieve what it was supposed to achieve but could do with a few minor tweaks which will be discussed in the next section and ways in which the Project could have been improved.

23. RECOMMENDATIONS

- A MOSFET can be used instead of a BJT. It has lower voltage drop.
- Provide better budget information and recommend suppliers for efficient component selection and purchasing with less delays.
- The use of a linear regulator (both an integrated circuit and a regulator built using passive components will do) will improve the output power quality of the SMPS.
- The use of a better filter after the rectifier stage to be able to further remove the ripples found after the rectifier.
- A cooling mechanism can be implemented to the design to present overheating.

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25. Appendix A - BILL OF MATERIALS

No.	Qtd	Descripti on	escripti Value Supply Manufac Supplier n Package turer		Supplier	Unit Price	Total Cost [R]	
				/Part Number			[R]	
1	1	Extension cord	-	34918	PowerWo rx	Builder s Supply	65.00	65.00
2	5	Diode, 400 V	-	1N539 5- E3/54GIC T-ND	Vishay Semicond uctor Diodes Division	Digikey .co.za	3.08	15.40
3	2	Capacitor , 450 V.	1000 uF	100UF 450VR	-	Communi ca.co.za	24.10	48.20
4	1	Mosfet	400 V	IRF740 BPBF	Vishay SiliConix	Digikey .co.za	23.15	23.15
5	1	Induct or. 1.6 A.	1 mH	811- 1343-ND	Murata Power Solutions Inc	Digikey .co.za	33.32	33.32
6	1	Capaci tor, Buck	10 µF	445- 8348-ND	TDK Corporati on	Digikey .co.za	6.02	6.02
7	2	NPN transistor s, 1 A	-	KSC50 27OTU- ND	ON Semicond uctor	DigiKey.c o.za	13.65	27.30
8	1	Resistor	100 Ω	PPC5W10 0TB-ND	Vishay BC Compone nt	DigiKey.c o.za	3.84	3.84
9	2	Digital Potentio meter. 8 bit.	1 kΩ	AD840 0ARZ1- ND	Analog Devices Inc	DigiKe y.co.za	44.29	88.58
10	1	Arduin o Uno Rev 3	-	ACM ARDUINO COMP UNO REV3	-	Comm unica.co.z a	146.0 0	146.0 0
11	1	UCT STM DEV board. [Already in possessio n]	-	-	UCT	UCT	-	0 [cost - 405]
12	1	Packaging costs	-	-	-	-	-	100
Total	costs			R	556.81			



26. Appendix B: Video of the first working prototype (double click to play)

Figure 43: First test

The following figure shows a sudden loading of the SMPS.



Figure 44:Sudden loading simulation results